This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor memory device comprising:

a first nonvolatile storage configured to store semiconductor chip codes of semiconductor chips;

a latch circuit configured to latch an address upon receipt of an activating signal; and

a first comparator circuit configured to compare a semiconductor chip code inputted from an external source with the semiconductor chip codes stored in the first storage, and output the activating signal when the inputted chip code coincides with one of the stored chip codes.

2. (Original) The semiconductor memory device according to claim 1, further comprising:

a write control circuit configured to generate a write signal; and

a second nonvolatile storage configured to store the address latched by the latch circuit upon receipt of the write signal.

3. (Original) The semiconductor memory device according to claim 2, further comprising:

a first memory cell array formed of a plurality of memory cells;

a second memory cell array formed of a plurality of redundancy cells;

an address buffer configured to receive an input address;

a second comparator circuit configured to compare the input address of the address buffer with the address stored in the second storage, and output an output signal denoting a coincidence/non-coincidence thereof; and

an output multiplexer configured to receive the output signal of the second comparator circuit and select data read out from one of the first and second memory cell arrays in accordance with the coincidence/non-coincidence denoted by the output signal of the second comparator circuit.

4. (Original) The semiconductor memory device according to claim 1, in which the first storage comprises memory cells in which the chip codes are re-storable.

5. (Original) The semiconductor memory device according to claim 2, in which the first storage comprises memory cells in which the chip codes are re-storable.

6. (Original) The semiconductor memory device according to claim 3, in which the first storage comprises the memory cells in which the chip codes are re-storable.

7. (Original) The semiconductor memory device according to claim 3, in which the second storage comprises the memory cells having a structure the same as the memory cells of the memory cell array, in which the address is re-storable.

8. (Original) The semiconductor memory device according to claim 1, further comprising:

a write control circuit configured to generate a write signal; and

a second nonvolatile storage configured to simultaneously store all address data latched by the latch circuit upon receipt of the write signal.

9. (Original) The semiconductor memory device according to claim 8, further comprising:

a first memory cell array formed of a plurality of memory cells;

a second memory cell array formed of a plurality of redundancy cells;

an address buffer configured to receive an input address;

a second comparator circuit configured to compare the input address of the address buffer with the address stored in the second storage, and output an output signal denoting a coincidence/non-coincidence thereof; and

an output multiplexer configured to receive the output signal of the second comparator circuit and select data read out from one of the first and second memory cell arrays in accordance with the coincidence/non-coincidence denoted by the output signal of the second comparator circuit.

10. (Original) The semiconductor memory device according to claim 8, in which the first storage comprises memory cells in which the chip codes are re-storable.

11. (Original) The semiconductor memory device according to claim 9, in which the first storage comprises memory cells in which the chip codes are re-storable.

12. (Original) The semiconductor memory device according to claim 9, in which the second storage comprises memory cells having a structure the same as the memory cells of the memory cell arrays, in which the address is re-storable.

13. (Original) The semiconductor memory device according to claim 1, in which the address latched by the latch circuit is an address of an area of a storing portion of each of the semiconductor chips, which area is faulty.